Modular, Fault-Tolerant Electronics Supporting Space Exploration, Phase II

Completed Technology Project (2006 - 2008)

Project Introduction

Modern electronic systems tolerate only as many point failures as there are redundant system copies, using mere macro-scale redundancy. Fault Tolerant Electronics Supporting Space Exploration (FTESSE) creates an electronic design paradigm using reprogrammable FPGAs to create swappable Circuit Object Blocks (COBs) -- analogous to software objects -- for the first time enabling redundancy on a micro-scale. The result is an increased tolerance of point failures by several orders of magnitude over traditional approaches. In the FTESSE approach, FPGAs are partitioned into COBs (groups of gates), each performing a specific function. Bad areas can be mapped like the bad sector data on a disk drive, enabling COBs to be placed in areas of working gates to recover system performance. Hardware tested during Phase I verified point failures could be introduced into an example circuit and corrected. As in the Phase I model, circuits to be monitored reside on a Slave FPGA, and a Master FPGA monitors outputs of all COBs, sensing faults and mapping non-working gates on the Slave FPGA. The Master is a rad-hard, triple mode redundancy (TMR) FPGA, but the Slaves need not be, opening the doors to higher performance applications while maintaining high levels of fault tolerance.

Primary U.S. Work Locations and Key Partners

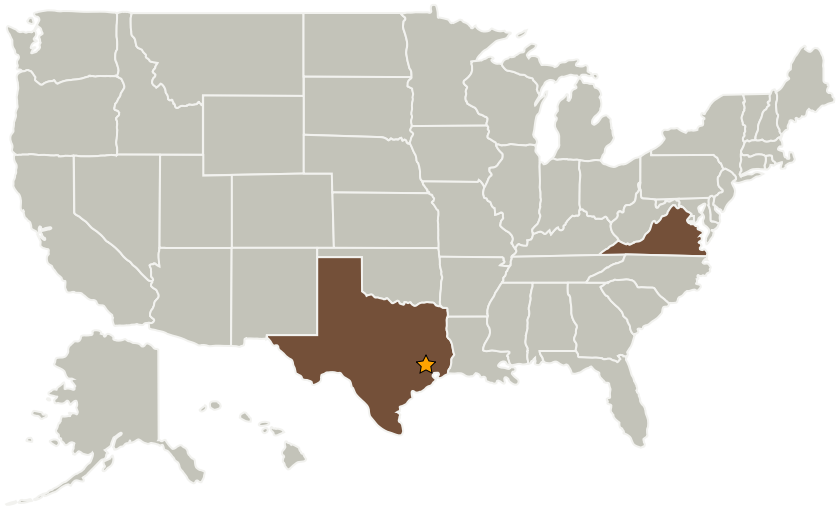

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Table of Contents

Organizational Responsibility

Responsible Mission Directorate:

Space Technology Mission Directorate (STMD)

Lead Center / Facility:

Johnson Space Center (JSC)

Responsible Program:

Small Business Innovation Research/Small Business Tech Transfer

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Organizations Performing Work	Role	Type	Location
★Johnson Space Center(JSC)	Lead Organization	NASA Center	Houston, Texas
AeroAstro Corporation	Supporting Organization	Industry	Ashburn, Virginia

Primary U.S. Work Locations	
Texas	Virginia

Project Management

Program Director:

Jason L Kessler

Program Manager:

Carlos Torrez

Technology Areas

Primary:

- TX02 Flight Computing and Avionics
  - TX02.1 Avionics Component Technologies
    - TX02.1.3 High Performance Processors